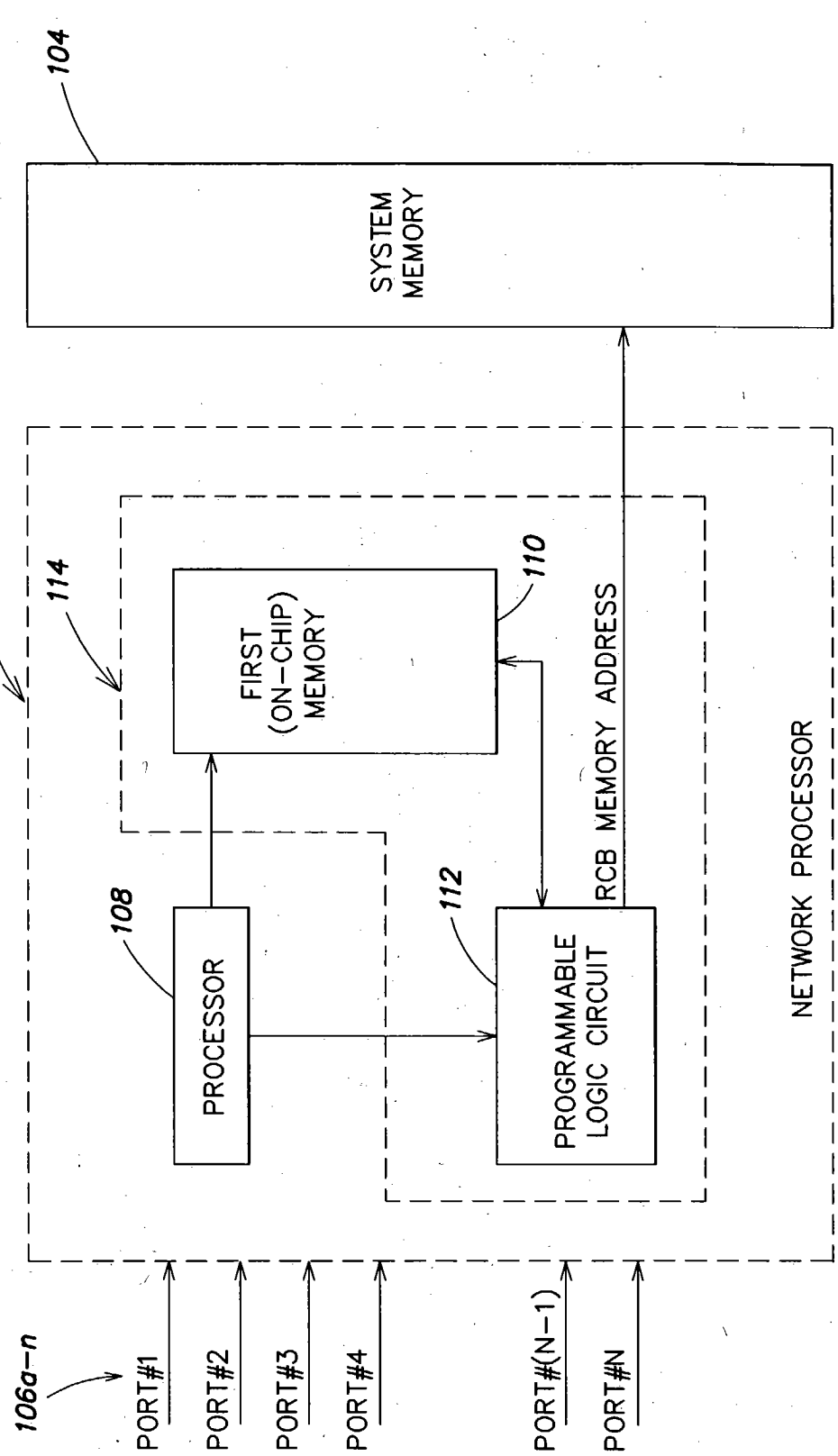
100
104
SYSTEM MEMORY
102
114
110
FIRST (ON-CHIP) MEMORY
RCB MEMORY ADDRESS
108
112
PROCESSOR
PROGRAMMABLE LOGIC CIRCUIT
NETWORK PROCESSOR
106a-n
PORT#1
PORT#2
PORT#3
PORT#4
PORT#(N-1)
PORT#N

FIG. 1

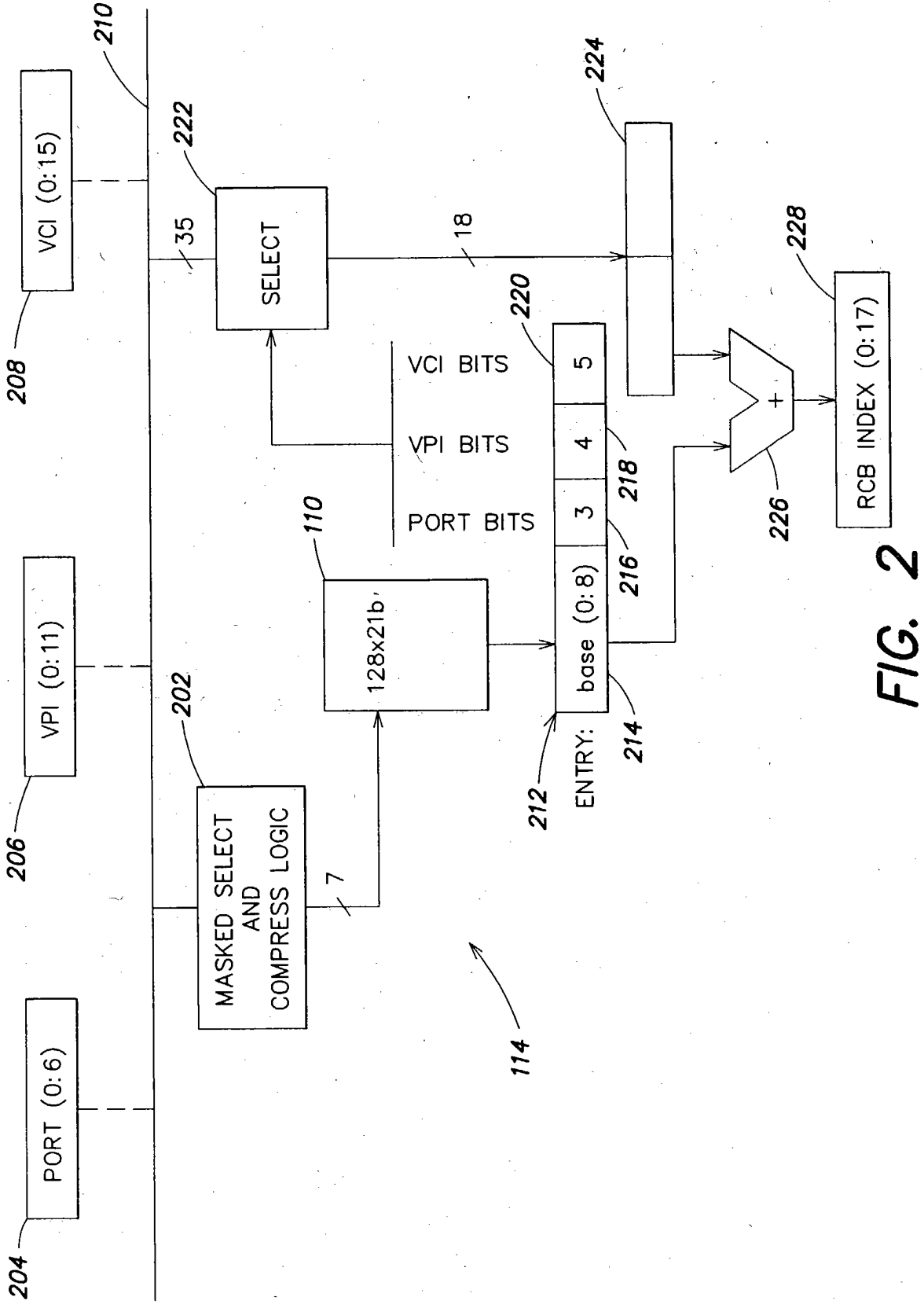
210
VCI (0:15)
208
222
SELECT
35
18
224
220
5
4
218
3
216
base (0:8)
214
ENTRY:
212
VCI BITS
VPI BITS
PORT BITS
110
128x21b
VPI (0:11)
206
202
MASKED SELECT AND COMPRESS LOGIC
7
PORT (0:6)
204
114
226
228
RCB INDEX (0:17)

FIG. 2

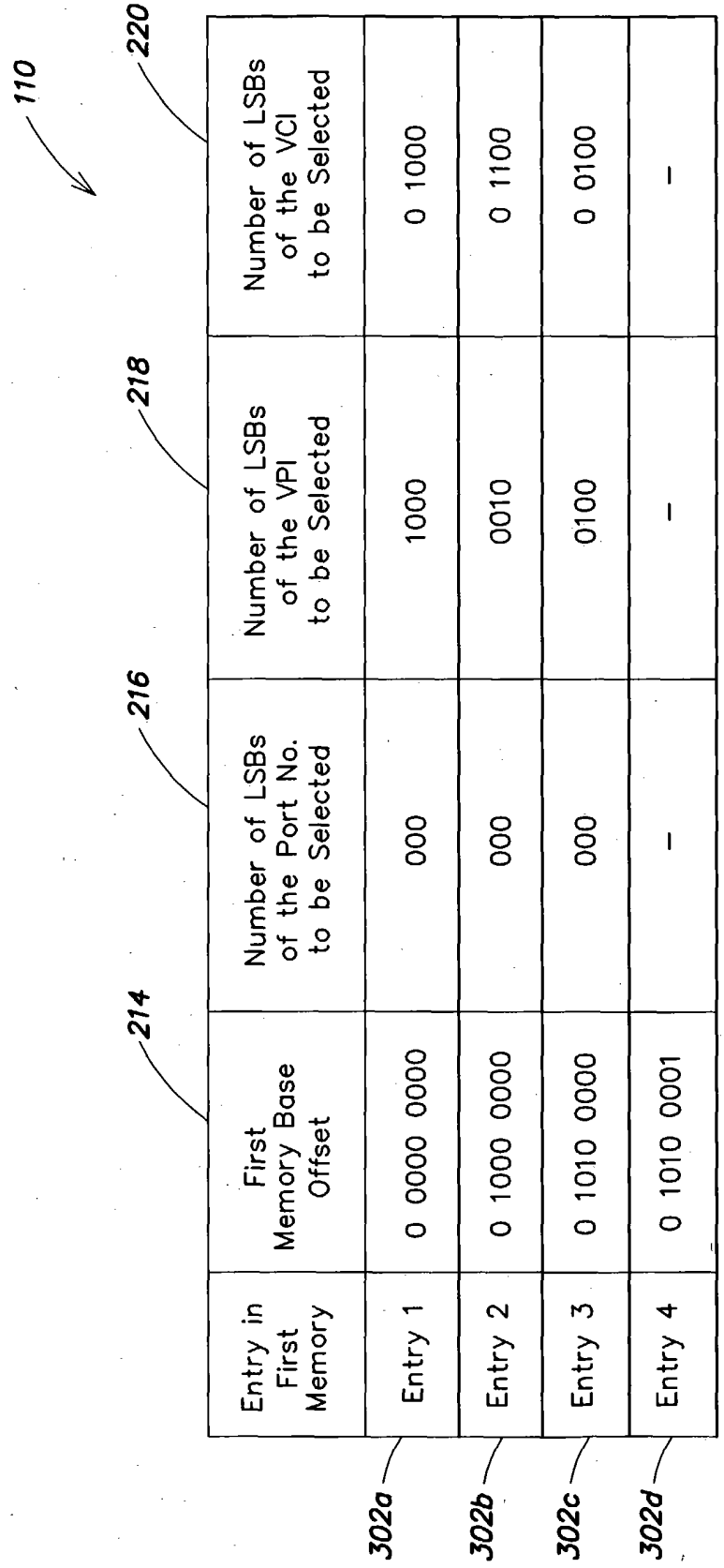
110
220
218
216
214
Entry in First Memory
First Memory Base Offset
Number of LSBs of the Port No. to be Selected
Number of LSBs of the VPI to be Selected
Number of LSBs of the VCI to be Selected
Entry 1
0 0000 0000
000
1000
0 1000
Entry 2
0 1000 0000
000
0010
0 1100
Entry 3
0 1010 0000
000
0100
0 0100
Entry 4
0 1010 0001
–
–
–
302a
302b
302c
302d

FIG. 3

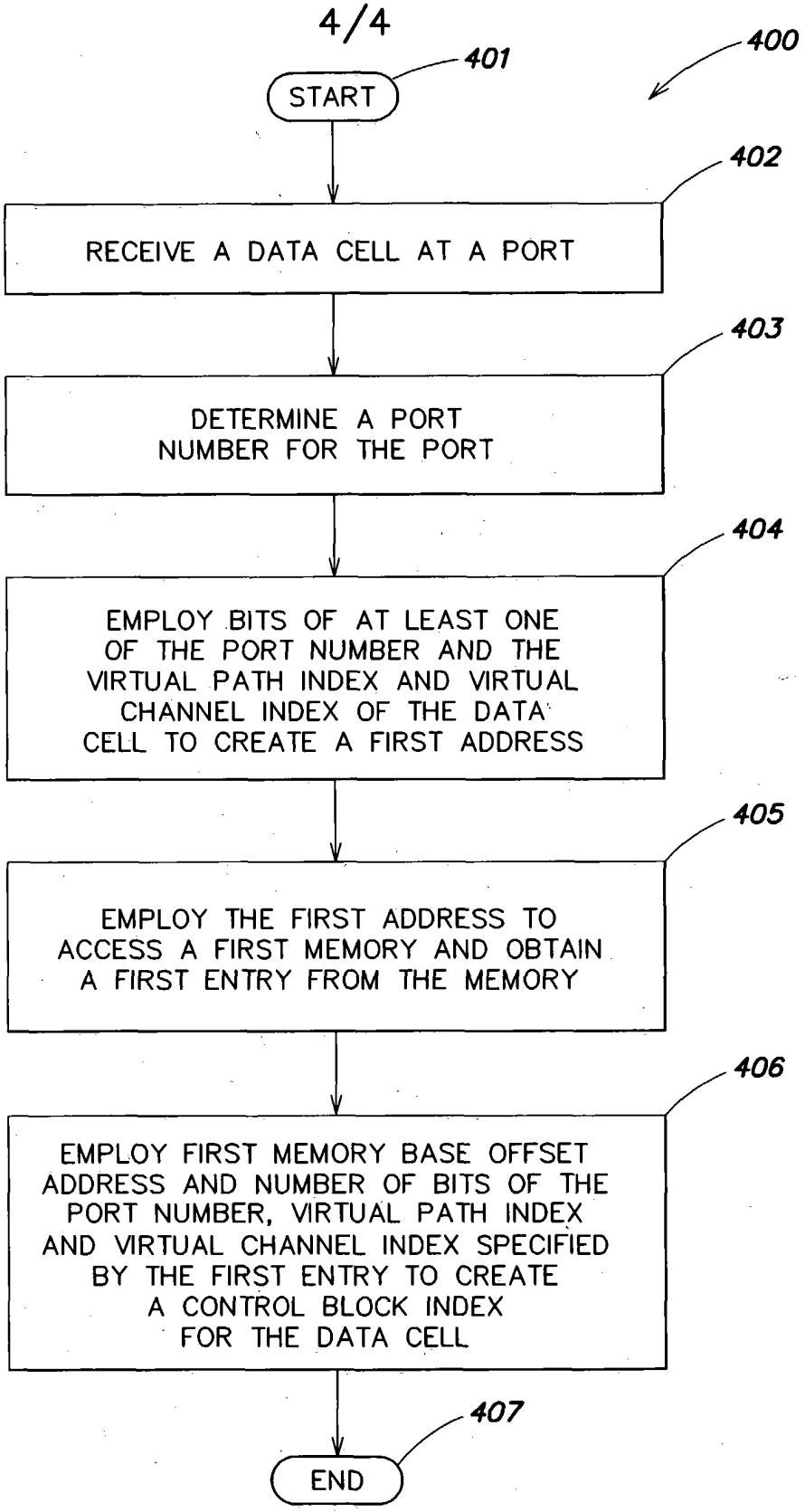
400
401
START
402
RECEIVE A DATA CELL AT A PORT
403
DETERMINE A PORT NUMBER FOR THE PORT
404
EMPLOY BITS OF AT LEAST ONE OF THE PORT NUMBER AND THE VIRTUAL PATH INDEX AND VIRTUAL CHANNEL INDEX OF THE DATA CELL TO CREATE A FIRST ADDRESS
405
EMPLOY THE FIRST ADDRESS TO ACCESS A FIRST MEMORY AND OBTAIN A FIRST ENTRY FROM THE MEMORY
406
EMPLOY FIRST MEMORY BASE OFFSET ADDRESS AND NUMBER OF BITS OF THE PORT NUMBER, VIRTUAL PATH INDEX AND VIRTUAL CHANNEL INDEX SPECIFIED BY THE FIRST ENTRY TO CREATE A CONTROL BLOCK INDEX FOR THE DATA CELL
407
END

FIG. 4